Standard Tests on Elementary Devices for Process Quality Characterization & monitoring

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INTRODUCTION

- ICs need close to 0ppm failure when used by customers
- To achieve this objective, quality must be high in all the steps of design & production
- Electrical Test at Wafer Level is one of the important steps that help to reduce the delay between the processing and the quality evaluation
- The purpose of this presentation is to introduce Standard Electrical Methods used to evaluate Quality and Reliability at Wafer Level and to explain the links with other means of Characterization (within Failure Analysis flow)

MAIN STANDARD METHODS

- **DIELECTRIC LAYERS**
  - Capacitance Voltage Characteristics
  - Triangular Voltage Stress or Bias Temperature Stress
  - Dielectric Leakage & Breakdown
- **METAL LAYERS**
  - Electro-migration
  - High Temperature Stress
- **SILICON**
  - Junction leakage, isolation & breakdown
- **DEVICES (process & layout effects)**
  - Transistors: Degradation by Hot Carriers
  - Memory cells: Data Retention, Cell Cycling
  - Antenna Structures: Process charging evaluation

Capacitance-Voltage Characteristics

- **MEASURE**: Capacitance for small dynamic signals at various DC biases is measured from silicon inversion to accumulation modes.
- **DEVICE:** Metal Oxide Semi-Conductor structures
- **OUTPUT PARAMETERS**: Oxide Thickness, Substrate Doping Level, Bulk & Interface Final Oxide Charges.
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - Spread-sheet resistance (doping profiles)
  - SIMS (bulk components and impurities levels)
  - TEM (thin oxide thickness, very local topology, .. 3D holography)
  - SEM or FIB (topology)
  - …

Triangular Voltage Stress / Bias Temperature Stress

- **MEASURE**: Change of characteristics (C-V or Threshold Voltage) due to temperature (>300°C) & bias is evaluated
- **DEVICE:** Metal Oxide Semi-Conductor or MIM structures (capacitances or transistors)
- **OUTPUT PARAMETERS**: Mobile Ion contamination
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - SIMS (bulk components and impurities levels)
  - ...

Leakage & dielectric Breakdown

- **MEASURE**: Dielectric is stressed (Current or Voltage, constant or ramped) up to a pre-defined level to check its characteristics of leakage, or up to its breakdown (non reversible state)
- **DEVICE:** Metal Oxide Semi-Conductor or MIM structures (capacitances or transistors) with large area and/or perimeters
- **OUTPUT PARAMETERS**: Oxide Strength (leakage parameters; breakdown parameters – critical electrical field & charge to breakdown; statistical data treatment)
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - Emission Microscopy (localization of defects)
  - SEM or FIB (topology)
  - TEM (morphology, … but also 3D holography, stress, …)
  - EDX (contaminants in particles)
  - SIMS (bulk components and impurities levels)
  - Failure analysis localization techniques : Liquid Cristal , EMMI, …
  - Scanning Capitance,microscopy, Tunelling AFM

Electro-migration

- **MEASURE**: Metal structure (generally simple line) is stressed under high current density stress (so that its temperature is elevated in the 200°C-300°C range) up to a resistance change (from 2% variation up to an open)
- **DEVICE:** Metal line or more complicated structure
- **OUTPUT PARAMETERS**: Medium Time To Failure and statistical distribution of failures
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - Advanced Optics
  - TEM, SEM or FIB (morphology, grain size & distribution)
  - EDX (components in particles)
  - OBIRCH
  - …

High Temperature Stress

- **MEASURE**: Resistance and Isolation between metal lines before and after temperature anneal
- **DEVICE:** Long metal lines (combs and snakes) intra or inter metal levels
- **OUTPUT PARAMETERS**: Shift of resistances, shorts and open (voiding or extrusion)
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - Advanced Optics
  - Emission Microscopy (localization of defects)
  - SEM or FIB (topology)
  - EDX (components in defects)
  - …

Junction leakage and breakdown, and isolation between junctions

- **MEASURE**: I-V characteristics of junctions (isolated or multi-junction environment) in reverse mode
- **DEVICE:** Structures with junctions to be studied present
- **OUTPUT PARAMETERS**: Breakdown Voltage and leakage current or corresponding voltage level
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - SEM or FIB (topology) with revelation of junctions
  - SIMS (bulk components and impurities levels)
  - Spreading resistance
  - …

Hot Carrier Injection

- **MEASURE**: Aging of transistors submitted to drain voltages larger than standard use with quantification of standard parameters shifts
- **DEVICE:** Transistors of each type with various dimensions and environments
- **OUTPUT PARAMETERS**: Threshold Voltage Shift, Driving Current shifts, Trans-conductance shift, Lifetime
- **COMPLEMENTARY ANALYSES on MATERIALS**:
  - SEM or FIB (topology)
  - TEM (topology)
  - SIMS (bulk components and impurities levels)
  - …

SUMMARY

- We have presented some Standard Electrical Methods used to characterize the quality of semi-conductor technologies. Let recall that Electrical Test at Wafer Level is very important to achieve quickly high quality, but has to be put in a Failure Analysis Flow
- Up-to-date equipments for complementary analyses are crucial (with Navigation Tools permitting direct positioning); main needs linked to Electrical Tests have been mentioned